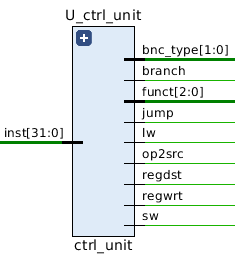
#### Control Unit

jx755

#### 1.1 inplementation

The control unit of the block diagram examines the instruction opcode bits [31 – 26] and decodes the instruction to generate control signals to be used in the additional modules.

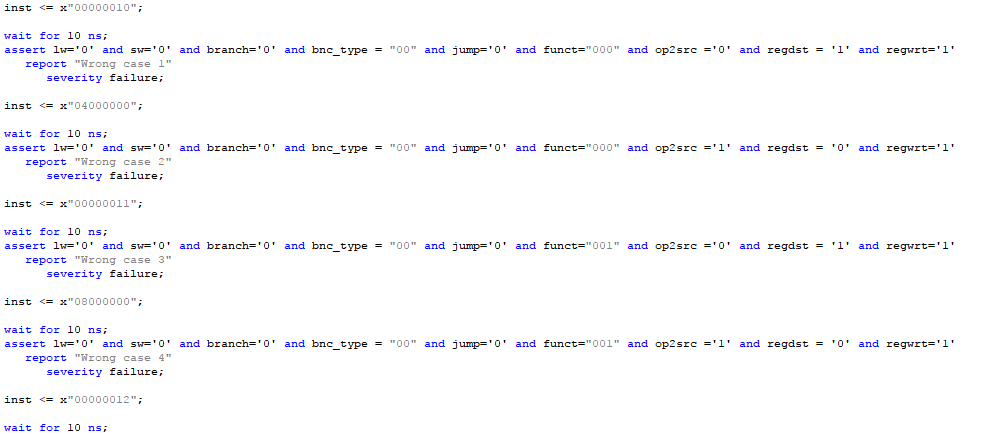
* lw : out STD\_LOGIC; HIGH when instruction is LW
* sw : out STD\_LOGIC; HIGH when instruction is SW
* branch : out STD\_LOGIC; HIGH when instruction is BLT | BEQ | BNE
* bnc\_type : out STD\_LOGIC\_VECTOR (1 downto 0); 01 when BNE; 11 when BEQ; 10 when BLT
* jump : out STD\_LOGIC; HIGH when instruction is JMP
* funct : out STD\_LOGIC\_VECTOR (2 downto 0); according to ALU operations
* op2src : out STD\_LOGIC; HIGH when instruction is I-type (except BXX)
* regdst : out STD\_LOGIC; HIGH when instruction is R-type
* regwrt : out STD\_LOGIC; HIGH when opcode == 00 to 07



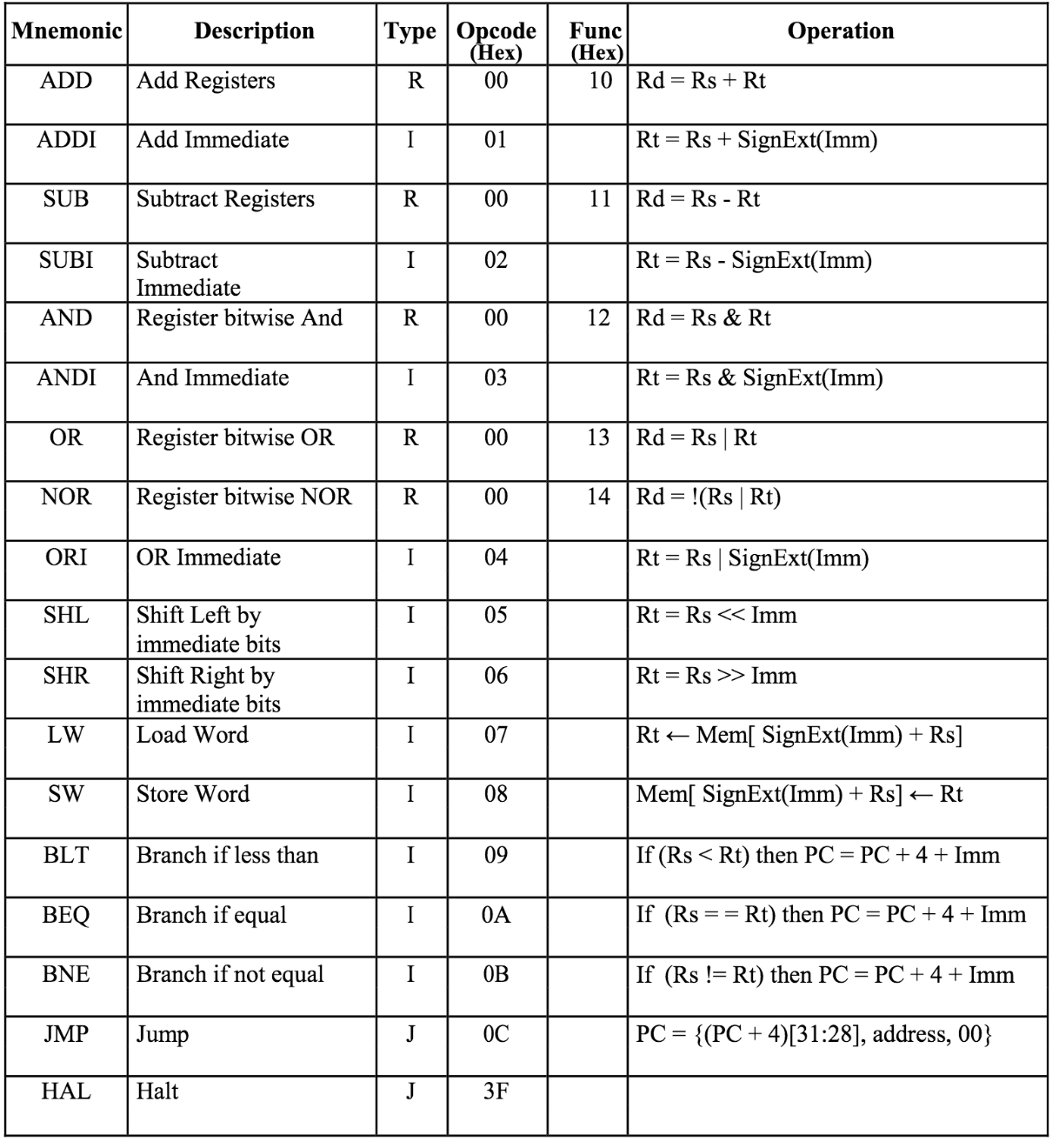
We tested all 18 instrutions and checked if the output controll signals are correct.

##### 1.2 testbench

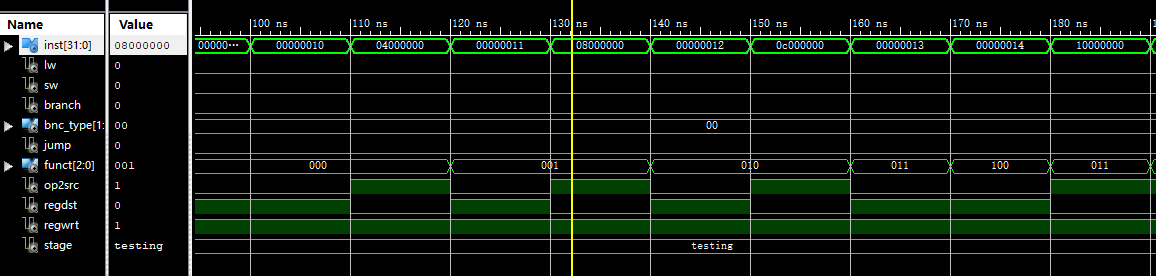
For each condition, I make one instruction to test correctness(bits unused is set to be zero) and used ‘assert’ statement to check the output automatically (see tb\_ctrl\_unit.vhd for details). The stage signal would change to FINISH only when all test cases passed, otherwise, the simulation would stop with severity level ‘failure’.



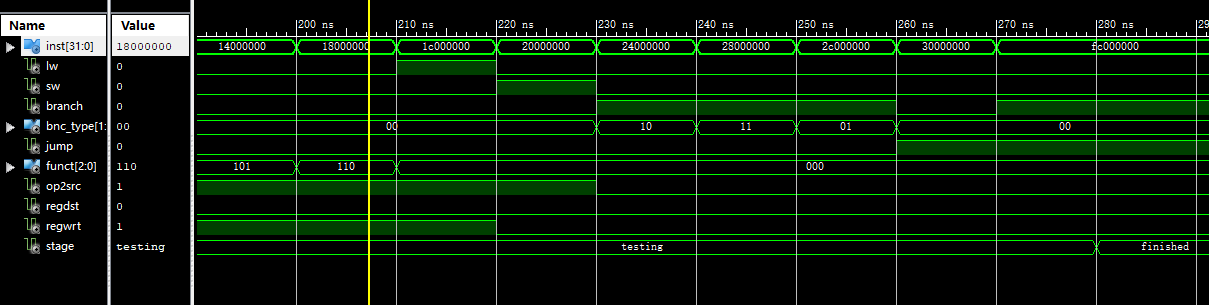
And the order of test instructionts are according to the instrucionts needed as:



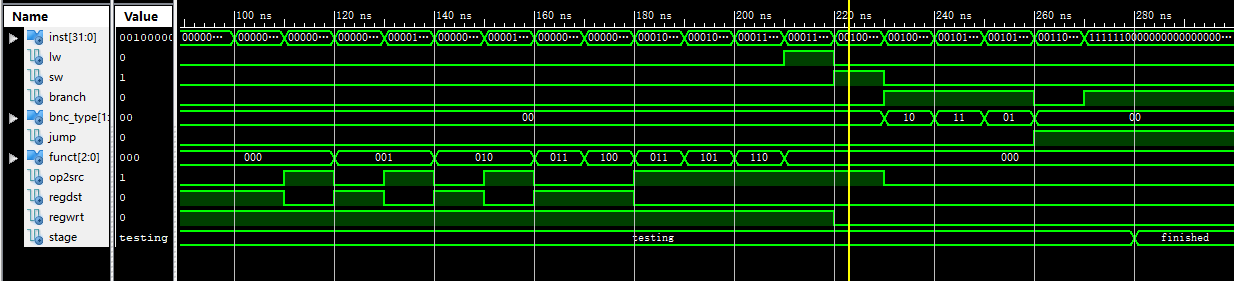
##### 1.3 Functional Simulation



1.3.1 Testing first 9 conditions

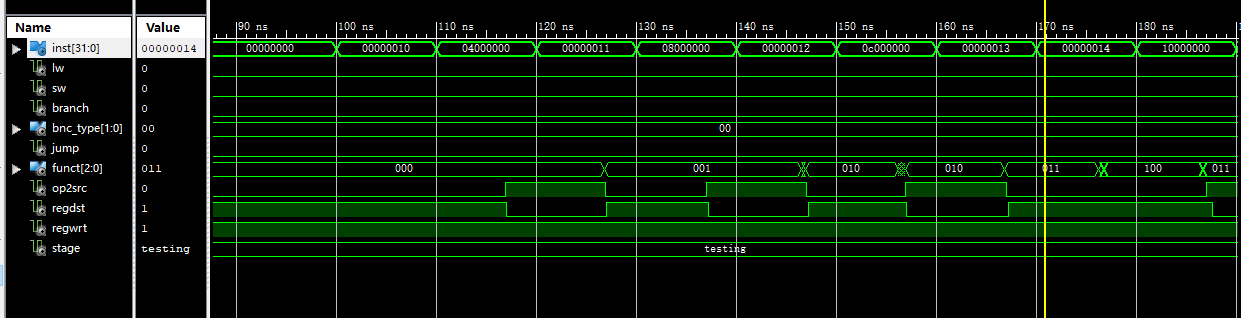


1.3.2 Testing latter 9 conditions

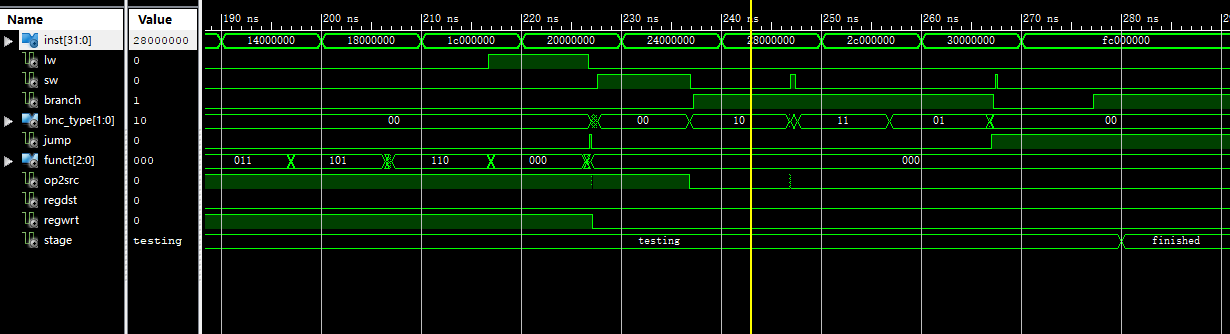


1.3.3 An overview with all cases passed.

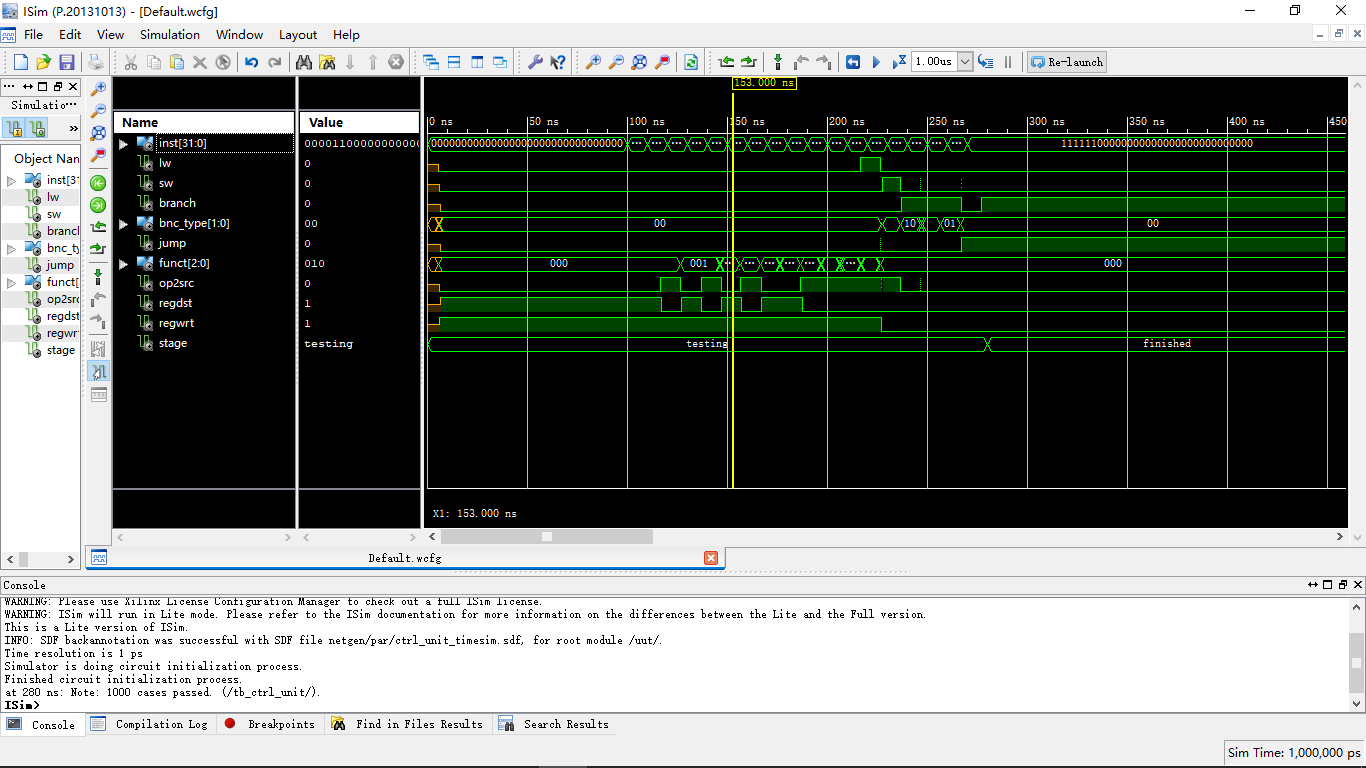
##### 1.4 Timing Simulation



1.4.1 Testing first 9 conditions



1.4.2 Testing latter 9 conditions



1.4.3 An overview with all cases passed.

1.5 timing analysis

|  |  |
| --- | --- |
| Critical path delay | 2.356 ns |
| Highest frequency | MHz |

Try many time after google, no timing report shows: The clock report is not displayed in the non timing-driven mode.